

### REMARKS

Applicants' remarks, below, are preceded by quotations of the related comments of the Examiner, in small, boldface type.

#### *Drawings*

1. **New corrected drawings are required in this application because in some instances letters and numbers are unreadable. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.**

Applicant submitted formal drawings on September 24, 2003, which Applicant believes corrects the deficiencies identified by the Examiner.

#### *Specification*

2. **Applicant is reminded of the proper content of an abstract of the disclosure. ...**

**The abstract should not refer to the purported merits or speculative applications of the invention and should not compare the invention with the prior art.**

....

**Extensive mechanical and design details should not be given.**

....

3. **Applicant is reminded of the proper language and format for an abstract of the disclosure. ...**

While Applicant does not believe that the previous abstract was defective, Applicant has amended the specification to include a new abstract consistent with the guidelines cited by the Examiner.

#### *Specification*

....

4. **The disclosure is objected to because of the following informalities:  
a. On page 7, line 6 – “a DC voltage source (say, between 1.5 and 100 volts, not shown) connected to an input 15”, but on Figure 3 that parameter is shown as 1.5-30 volts.  
b. On page 7, line 20 – “the control circuit 24 provides three primary functions”, but on line 16 and Figure 4 number 25 is assigned to a body diode and the control circuit is numbered as 25.  
Appropriate correction is required.**

Applicant thanks Examiner for identifying these informalities and has amended the specification to make the appropriate corrections.

*Information Disclosure Statement*

Note that an applicant's duty of disclosure of material and information is not satisfied by presenting a patent examiner with "mountain of largely irrelevant [material] from which he is presumed to have been able, with his experience and with adequate time, to have found the critical [material]. It ignores the real world conditions under which examiners work." .... Patent applicant has a duty not just to disclosure pertinent prior art references but to make a disclosure in such as way as not to "bury" it with other disclosures of less relevant prior art ... .

Although Applicant appreciates the Examiner's comments, Applicant has attempted to comply with its duty of disclosure under 37 C.F.R. 1.56 in good faith by submitting all information known to be material to patentability. The Federal Circuit has emphasized that "when a question of materiality is close, a patent applicant should err on the side of disclosure." *LNP Eng'g Plastics, Inc. v. Miller Waste Mills, Inc.*, 275 F.3d 1347 (Fed. Cir. 2001); *see also*, *Brasseler, U.S.A. I, L.P. v. Stryker Sales Corp.*, 267 F.3d 1370 (Fed. Cir. 2001) ("To avoid a finding of inequitable conduct, doubts concerning whether information is material should be resolved in favor of disclosure."); *see, also* MPEP §2004 ¶10("When in doubt it is desirable and safest to submit information."). Accordingly, Applicant has erred on the side of disclosing references which Applicant believes may be material to patentability and has not made any attempt to "bury" what Applicant perceives as a particularly relevant reference amongst several marginally relevant references.

*Claim Rejections – 35 USC §103*

5. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marusik (5,945,816) in view of Black et al. (5,009,618). Marusik disclosed a self-biased power isolator system, comprising two or more electronic components (Fig. 4, Pos. 120, 160) having: an internal circuit having a controlled element (120 or 160) and control element (50 or 90), the internal circuits are connected in parallel to common point (node 2) to supply power and cooperatively protect the external circuit against occurrence of an adverse electrical event wherein none of the electronic components has rating sufficient by itself to protect the external circuit (load 18). Marusik disclosed that "the first node is operable to be coupled to a power supply 10 and the second node is operable to be coupled to load 18" (Abstract). All of the internal circuits, as similar and therefore should be manufactured as a replaceable blocks. It is well known in the art (Kirchoff's 1<sup>st</sup> law) that the current flowing (sic) from

node 2 through the load (18) will be equal to sum of current flowing (sic) from element 120 and current flowing (sic) from element 160. If, as Marusik suggested, N identical circuits will be installed, each node will experience  $1/N$  of the load current and therefore will need less rating of the elements.

Marusik is silent about types of the terminals coupled to the internal circuits, Black et al. teach a method and apparatus for making electrical connecting device where an "edge board connector is one which is mounted on one printed circuit board, and having contacts that are electrically connected to printed circuits on that printed circuit board and are electrically connectable to terminal pads of another printed circuit board to facilitate so called mother board-daughter board arrangements." It would have been obvious to one of ordinary skill in the art at the time [of] the invention to modify Marusik with Black et al. teachings and make all of the internal circuits as identical, easily replaceable surface mounted daughter-boards.

...

Amended claim 1 requires that the internal circuit occurrence of protect "the external circuit from drawing more than a threshold amount of current." Marusik describes circuitry for providing uninterrupted power to an external circuit (i.e., load 18 in Fig. 4) by controlling the connections between multiple power supplies (i.e., elements 10, 14) and the external circuit based on the relative voltages between at the output of the power supplies and the input of the external circuit. However, Marusik does not describe any circuitry for protecting the external circuit from drawing an threshold amount of current. Indeed, if the external load in Marusik were to short to ground (thus causing the external circuit to draw an excessive amount of current), Marusik does not describe any circuitry for cutting off current to the external circuit.

Applicant respectfully submits that claim 1 is patentable for at least these reasons. Dependent claims 2-12 depend from claim 1 and are therefore also patentable for at least the same reasons.

*Claim Rejections – 35 USC §103*

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6. Claims 25-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Notaro et al. (5,781,390). Notaro et al. disclose an integrated supply protection circuit comprising terminals for connecting the protection circuit respectively to a power source (Fig. 1, Pos. 115) and external circuit (120) that is to be powered by the source and protected by the protection circuit against occurrence of an electrical event. The protection circuit is connected to provide two different kinds of protection (a reverse battery condition and an overvoltage condition) using two controlled elements (140 and 145). ....

Amended claim 25 requires, among other things, "a first and second protection mechanism ...wherein the first protection mechanism provides a current drain on the power source to pull the voltage down at a point of load." Notaro does not describe such a circuit. While Notaro describes a protection circuit that provides overvoltage protection for an external circuit and reverse battery protection for a power source, Notaro's circuit does not provide any mechanism to provide a current drain on the power source to pull down the voltage at a point of load. Rather, in the event of a reverse battery condition, Notaro's circuitry simply disconnects the voltage source (V<sub>batt</sub> 115) from the external circuit. (See, Notaro 3: 51-56). In the case of an overvoltage condition, Notaro's circuitry is designed to cause the second MOSFET (i.e., MOSFET 145) to absorb the voltage transient. (See, Notaro 4: 20-27). Nowhere does Notaro suggest providing a current drain on the power source to pull down the voltage at a point of load.

Applicant respectfully submits that claim 25 is patentable for at least these reasons. Dependent claims 26-36 depend from independent claim 30 and are patentable for at least the same reasons.

*Allowable Subject Matter*

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7. Claims 13-14 and 35-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 14-15 (sic) are allowable because none of the prior art of record disclose an apparatus for protecting an external circuit against occurrence of an adverse electrical event in which the internal circuit includes elements adapted to pull up a voltage at one of the terminals when the voltage at the terminal drops and elements adapted to pull down the voltage at one of the terminals when the voltage at the terminal rises in combination with the other claim limitations.

Claims 35-36 are allowable because none of the prior art of record disclose an apparatus for protecting an external circuit against occurrence of an adverse electrical event in including an energy reservoir at a predetermined voltage, and in which the protection mechanism shunts current to the energy reservoir in combination with the other claim limitations.

Applicant thanks the Examiner for indicating that these claims are allowable.

Applicant has amended claim 13 and 14 to place in independent form and has included all of the limitations of original claims 13-14 except for the limitation that "none of the electronic components has ratings sufficient by itself to protect the external circuit." This limitation has

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been incorporated as a dependent claim in new claim 40. Applicant believes that the removal of this limitation from original claim 13 and 14 does not affect its patentability over the prior art.


Applicant has rewritten original claim 35 and 36 in independent form as new claims 41 and 42 respectively.

For at least the above reasons, Applicant respectfully submit that all pending claims are patentable. Please note that the fact that the Applicant has addressed certain comments of the Examiner does not mean that the applicant concedes any other positions of the Examiner. The fact that the Applicant has asserted certain grounds for the patentability of a claim does not mean that there are not other good grounds for patentability of that claim or other claims.

Enclosed is a \$226.00 check for excess claim fees and a \$110 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 1/12/04

  
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